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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
09/994,284	11/26/2001	Sang Jek Lee	CU-2636 VE	8830

26530 7590 03/25/2003

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EXAMINER
PHAM, THANH V

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,284	LEE ET AL.	
	Examiner	Art Unit	
	Thanh V Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-6 and 8-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/15/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (in combination with Maniar et al. U.S. Patent No. 5,356,833) and the following.

The applicants' admitted prior art as explained in figures 1 and 2 and the background of the invention has a method of forming a gate in a semiconductor device *having a non-linear top profile (that is not different from the detailed description of the preferred embodiments referring to FIG. 3A to 3F), the method* comprising the steps of:

forming a dummy gate insulating layer 2 on a semiconductor substrate 1 having a field oxide layer isolating the device (not shown, page 3, lines 13-14); depositing a dummy gate polysilicon layer 3 and a hard mask layer 4 on the dummy gate insulating layer 2 sequentially; patterning the hard mask 4 into a mask pattern 4a and patterning the dummy gate polysilicon layer 3 *and the dummy gate insulating layer* using the mask pattern as an etch barrier *to create a plurality of patterned dummy gate polysilicon and insulating layers each having sidewall, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer*; forming spacers 6 at *the* sidewalls of the *patterned* dummy gate polysilicon 3 *and insulating layers*; depositing an insulating interlayer 7 on the resultant structure 5 after forming the spacers 6; exposing a surface of the *patterned* dummy gate polysilicon *and insulating* layers by carrying out an oxide layer CMP process, page 4, line 14, *using a first selection ratio sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers*; forming a damascene structure by removing the *patterned* dummy gate polysilicon *and* insulating layers using the insulating interlayer as another etch barrier, fig. 1D, page 4, lines 15-16 and page 5, lines 1-3; depositing a gate insulating layer 8 and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure, fig. 1E; and exposing a surface of the insulating interlayer by carrying out a metal chemical mechanical polishing process *using a second selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer, the 'wave-like' profile of the top of the gates is inherently formed again*.

The metal CMP uses slurry for a metal layer, page 13, lines 6-19.

In explaining the prior art, the applicants displays only one gate in fig.'s 1; however, with respect to fig. 2, line A-A' shows the potentially non-linearity of the tops of the gates (as in figures 3D and 3F).

In the description of applicant's admitted prior art the applicant does not state the thickness of the dummy gate polysilicon layer or the insulating interlayer, the polishing selection ratios between the insulating interlayer and the dummy gate polysilicon layer is over 20 or the gate metal layer is over 50, the using of CeO_2 and its pH between 3 and 11 in the insulating interlayer CMP and the pH between 2 and 7 of the slurry in the metal layer CMP.

Choice of 1,300 to 2,000 angstroms for the gate layer and 4,000 to 5,000 angstroms for the interlayer to achieve particular device properties would have been a matter of routine optimization because the thickness is known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics.

Maniar et al. reference discloses use of CeO_2 as slurry in CMP oxide removal process in the variation of topologies with a pH in a range of about 2-5 or the pH outside the range may be used (col. 4, lines 23-40 and col. 5, line 57 to col. 6, line 29). *Moreover,* with the confirmation of applicants' argument that the CMP slurry disclosed in the cited Maniar et al. reference is one of a number of materials well known in the art (paper #7, page 3, line 1, filed 12/03/03), the recited selection ratios would be obtained

in the process of the combination because the same *known* materials are treated in the same manner as in the instant invention.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V Pham whose telephone number is 703-308-2543. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TvP

TvP
March 21, 2003

George Fourson
Primary Examiner
2823